



**Shri Vaishnav Vidyapeeth Vishwavidyalaya**  
**Shri Vaishnav Institute of Technology and Science**  
**Choice Based Credit System (CBCS) Scheme in the light of NEP-2020**

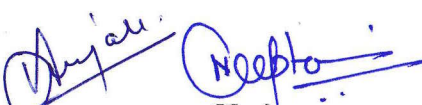
**B.Tech. in Electrical and Electronics Engineering (Semiconductor Chip Design and VLSI for Industrial Applications in Collaboration with L&T Edutech)**

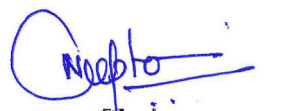
**SEMESTER-I (2025-2029)**


S. No.	COURSE CODE	COURSE NAME	TEACHING SCHEME/WEEK			CREDITS	EXAMINATION SCHEME					TOTAL MARKS
			L	T	P		THEORY			PRACTICAL		
							End Sem University Exam (60%)	Two Term Exam (20%)	Teachers Assess-ment* (20%)	End Sem University Exam (60%)	Teachers Assess-ment* (40%)	
1	BTEE106	Fundamentals of Electrical and Electronics Engineering	3	0	2	4	60	20	20	30	20	150
2	BTME101	Engineering Drawing	1	0	4	3	60	20	20	30	20	150
3	BTEC104	Digital Logic and Circuit Design	3	1	2	5	60	20	20	30	20	150
4	BTVDLT101	IT Primer	2	1	0	3	60	20	20	0	50	150
5	BTMA101N	Mathematics I	3	1	0	4	60	20	20	0	0	100
6	HUCS101	Communication Skills	1	0	2	2	60	20	20	0	20	120
6	BTCS101	Computer Programming I	0	0	2	1	0	0	0	30	20	50
TOTAL			13	3	12	22	360	120	120	120	150	870

**Legends: L - Lecture ; T - Tutorial/Teacher Guided Student Activity ; P - Practical**

**\*Teacher Assessment shall be based on following components: Quiz/Assignment/Project/Participation in Class, given that no component shall exceed more than 10 marks.**

  
**Chairperson**  
 Board of Studies  
 Shri Vaishnav Vidyapeeth  
 Vishwavidyalaya, Indore

  
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 Faculty of Studies  
 Shri Vaishnav Vidyapeeth  
 Vishwavidyalaya, Indore

  
**Controller of Examinations**  
 Shri Vaishnav Vidyapeeth  
 Vishwavidyalaya, Indore

  
**Registrar**  
 Shri Vaishnav Vidyapeeth  
 Vishwavidyalaya, Indore

  
**Vice Chancellor**  
 Shri Vaishnav Vidyapeeth  
 Vishwavidyalaya, Indore